STT Fake Data Generator

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Overview

A Fake data generator was implemented for use with DFEC board in the test stand located in FCH3. The board uses a 53MHz clock from a data pump, which is transmitted to the board through a LVDS cable into the link2 connection. The outputs are sent to the two G-link transmitters in slot 4. The fiber cables are routed to MCH2. The SMT data uses the top transmitter in 16 bit mode. Track data uses the L3_OUT bus, which feeds the bottom G-link transmitter in 20 bit mode. The event is repeated every 1 sec. In MCH2 the cables are grey(CFT) and orange(SMT). The *stttest.bit* file was downloaded to the 4^{th} slot in the FCH3 test stand via the JTAG interface. In the future, I will implement the download using a compact flash card.

A fake event was taken from the L2STT Monte Carlo, where a 50 GeV muon was simulated at phi=82.5 degrees.

CFT Data

The track hits CFT sector=17/fiber doublet=22, and the L2 trigger produces the following output stream.

```
...
F0 0000
F0 0000
B5 0301
B0 1110
B0 01A2
B0 FFFF
B0 0000
B0 0000
B0 0114
B0 3C02
B0 A201
BA 735B
F0 0000
F0 0000
...
```

where bits [0:19] are reversed in the transmitted data and F00000 are filler words. Bits [17:23] are G-link controls.

SMT Data

SMT data is delayed by ~5us with respect to the CFT data. The SMT data consists of 7 hits to form a cluster with centroid at (6.7101, 0.883403, 2.22355) cm. The hits are in Crate=0,HDI=5, and Chip=4 with

hit	chan	data
1	2	8
2	3	11
3	4	29
4	5	11
5	6	15
6	7	11
7	8	11

The HDI corresponding to bits [0:7] is given the index 4, however, the cluster in HDI index 5 is repeated.

This produces the following data stream

```
...
F0 C0C0 - fill
F0 C0C0 - fill
B0 0505 - seq
B0 0504 - hdi
B0 8484 - chip
B0 0000 - zero
B0 0202 – chan 1
B0 0808 – data 1
B0 0303 – chan 2
B0 0B0B – data 2
B0 0404 – chan 3
B0 1D0D – data 3
B0 0505 – chan 4
B0 0B0B – data 4
B0 0606 – chan 5
B0 0F0F – data 5
B0 0707 – chan 6
B0 0B0B – data 6
B0 0808 – chan 7
B0 0B0B – data 7
B0 C0C0 - fill
B0 C0C0 - fill
F0 C0C0 - fill
F0 C0C0 - fill
F0 C0C0 - fill
...
```

where bits [0:19] are reversed in the transmitted data and F0C0C0 are filler words.

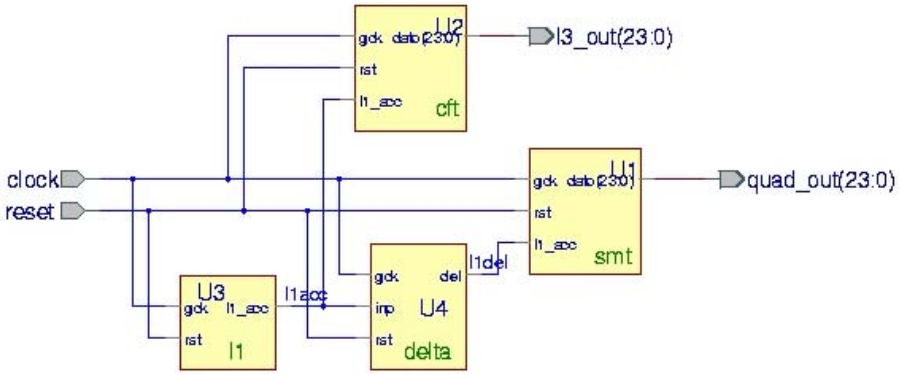
VHDL

The design is a block diagram called stttest.bde. This entity has two inputs: clock and reset signals. The two outputs are quad_out(SMT) and l3_out(CFT). Stttest connects four processes which are finite state machines:

- L1.vhd – generates a pulse every 10 seconds
- Delta.vhd – delays the l1acc signal by ~5us
- Cft.vhd – stores and outputs cft data
- Smt.vhd – stores and outputs smt data

The top level testbench is called tb.vhd. It is configured and executed by

- Tb_beh_cfg.vhd and tb_beh.do for functional simulations, and
- Tb_tim_cfg.vhd and tb_tim.do for timing simulations.



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Created:	3/8/2001
Title:	STTTest

Synthesis

From the Design Flow Manager -> synthesis options-> Run Mode: ->choose GUI and Top Level Unit: choose *stttest* from the pulldown menu.

Choose synthesis and FPGA Express will start and open a window.
The left window will have a file structure *stttest->WORK->all-design-files.vhd.*
Choose *stttest* and then SYNTHESIS->update.

From the pull-down menu choose *stttest* as the top level design
A box will open. Set clock frequency to 53 MHz and uncheck [ ]skip constraints.

From pull down menus choose: Vendor(Xilinx), Device(V600BG560), Speed(-5) and Family(VIRTEX). OK.

A chip will be created in the right window called *stttest.*
Choose the chip. From the high level menu choose SYNTHESIS->edit constraints->ports->Use I/O Reg->true
Global Bufer-> BUFGP for clocks
Close
Choose chip
SYNTHESIS->Optimize chip
SYNTHESIS->Export Netlist
Exit

Implementation

From the Flow Manager -> implement options->GUI
Brouse to find the Netlist file *c:/My_Designs/stttest/synthesis/stttest.edf*. OK.

Choose *implement*. A box will open saying that the synthesis is not up to date… and choose NO.
A window will open with a box for the constraints file. Choose custom and brouse to find the configuration file *c:/My_Designs/stttest/src/u5_pins.cfg*
Design->options->
Implementation: edit options->optimize and map -> Pack I/O Reg -> Inp and Out. OK.
Set part if necessary.
Simulation: edit options->sim data options->Active VHDL
Configuration -> JTAG
edit options->readback [X} Enable readback
OK. OK.
Design->Implement
Exit.

Data Formats

CFT data Format

23-20	19-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bits
glink	cont	headers, data, trailer																type
F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	blank
B	5	header length=03								number of objects								head 1
B	0	header format			object format					object length=??								head 2
B	0	bunch number								data type=A2-A5								head 3
B	0	rotation number																head 4
B	0	algorithm minV								algorithm maxV								head 5
B	0	status								process ????								head 6
B	0	S	Pt bin		Ext Pt			HPS	LPS	error code		R		PSC RA				track data
B	0	relative phi =1-44						ISO	eIS	D	TK sector address = 1-80							track data
B	0	data type=A2-A5								bunch number								trailer 1
B	A	longitudinal parity																trailer 2
F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	blank
F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	blank

Note: bits [0-15] are reversed before transmission

SMT data Format

23-20	19-16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	bits
glink	cont	headers, data, trailer																type
F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	blank
B	0	Sequencer ID								Sequencer ID								Seq
B	0	status					HDI ID			status					HDI ID			HDI
B	0	chip ID								chip ID								Chip
B	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	zero
B	0	channel #								channel #								cahn
B	0	data								data								adc
B	0	C0								C0								EOR
B	0	C0								C0								last
F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	blank
F	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	blank

Note: bits [0-15] are reversed before transmission